SRI KRISHNA COLLEGE OF ENGINEERING AND TECHNOLOGY COIMBATORE-8

(An Autonomous Institution Affiliated to Anna University Chennai)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

M.E (APPLIED ELECTRONICS)

AUTONOMOUS CURRICULUM AND SYLLABUS

REGULATIONS 2015

(For students admitted during 2015-16 and onwards)

From the academic year 2016 - 2017

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VISION

To be a center of excellence for technological education, training & Research and to produce world class Engineers who can be placed in top core companies to serve the nation and the society.

MISSION

- To provide intensive training in the fundamentals as well as the current trends in the field of Electronics and Communication Engineering.
- To continuously update the various facilities in the department and facilitate R&D and Consulting activities.
- To provide placement assistance to the students.
- To disseminate the knowledge by organizing seminars, Faculty Development Programs and Workshops.

SRI KRISHNA COLLEGE OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
REGULATION 2015
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CURRICULUM FOR M.E (APPLIED ELECTRONICS)

SEMESTER I							
S No.	**Course Code**	**Course**	**L/T/P**	**Contact hrs/week**	**Credit**	**Ext/Int**	**Category**
1	15PH203	Applied Mathematics for Electronic Engineers	3/2/0	4	4	60/40	FCBS
2	15PL401	Statistical Signal Processing	3/2/0	4	4	60/40	PC
3	15PL402	Advanced Digital Systems Design	3/2/0	4	4	60/40	PC
4	15PL403	VLSI Design Techniques	3/0/0	3	3	60/40	PC
5		PE – 1	3/0/0	3	3	60/40	PE
6		PE – 2	3/0/0	3	3	60/40	PE
7	15PL451	Advanced VLSI Laboratory	0/0/3	2	2	40/60	PC Lab
			Total	**23**	**23**	**700**	

SEMESTER II							
S No.	**Course Code**	**Course**	**L/T/P**	**Contact hrs/week**	**Credit**	**Ext/Int**	**Category**
1	15PL404	Analog Integrated Circuit Design	3/2/0	4	4	60/40	PC
2	15PL405	Digital Control Engineering	3/2/0	4	4	60/40	PC
3	15PL406	Embedded Systems Design	3/2/0	4	4	60/40	PC
4		PE - 3	3/0/0	3	3	60/40	PE
5		PE – 4	3/0/0	3	3	60/40	PE
6		PSC – 1	3/0/0	3	3	60/40	PSC
7	15PL452	Embedded Systems Laboratory	0/0/3	2	2	40/60	PC Lab
8	15PL801	Technical Seminar	0/0/2	2	1	40/60	
			Total	**25**	**24**	**800**	

FCBS - Foundation Compulsory Basic Science
PE - Programme Elective
PC - Programme Core
PSC - Programme Soft Core

SEMESTER III							
S No.	Course Code	Course	L/T/P	Contact hrs/week	Credit	Ext/Int	Category
1		PSC – 2	3/0/0	3	3	60/40	PSC
2		PE – 5	3/0/0	3	3	60/40	PE
3		PE – 6	3/0/0	3	3	60/40	PE
4	15PL901	Project Work & Viva-voce – Phase I	0/0/12	12	6	40/60	Project
5	15PL802	Comprehensive Viva – Voce	0/0/2	2	1	40/60	
			Total	**23**	**16**	**500**	

SEMESTER 4:

SEMESTER IV							
S No.	Course Code	Course	L/T/P	Contact hrs/week	Credit	Ext/Int	Category
1	15PL902	Project Work & Viva-voce - Phase II/Internship	0/0/24	24	12	40/60	Project
			Total	**24**	**12**	**100**	

PE - Programme Elective PSC - Programme Soft Core

Program Elective (PE) Groups:

S.No	SUB CODE	Group Name	List of subjects
1	15PL601	Embedded Systems	High performance microprocessors and microcontrollers
	15PL602		RTOS and its Applications
	15PL603		Embedded C
2	15PL604	VLSI	CAD of VLSI Circuits
	15PL605		Testing of VLSI Circuits
	15PL606		System on Chip design
3	15PL607	Device Modeling	MEMS and its Applications
	15PL608		Nano Electronic Devices
	15PL609		Solid State Device Modeling and Simulation
4	15PL610	Instrumentation and Control	Electronic Instrumentation
	15PL611		Fault Tolerant Systems
	15PL612		Non-Linear Control System
5	15PL613	Advanced Design	RF System
	15PL614		Signal Integrity for high speed design

	15PL615		Electromagnetic Interference and Compatibility

Program Soft Core (PSC) Group

S.No	SUB CODE	Subject Name
1	15PL501	Principles of Soft Computing
2	15PL502	Design of Low Power VLSI circuits
3	15PL503	Design of Application Specific Integrated Circuits
4	15PL504	Hardware Software Co-design
5	15PL505	Reconfigurable Computing

Note :

1. **Programme Electives (PE) must be framed by having 5 domains, each possessing 3 subjects. Students should get specialized in any two domains.**
2. **List of subjects must be given in Programme Soft Core (PSC), so that students can choose any 2 subjects.**
3. **Students can earn extra credits by doing certification courses.**

Curriculum Structure

S.No	Category Name	Credits Break Up
1	Foundation Compulsory Basic Science (FCBS)	4
2	Programme Core(PC)	23
3	Programme Elective(PE)	18
4	Programme Core(PC) Lab	4
5	Programme Soft Core(PSC)	6
6	Project	18
7	Technical Seminar	1
8	Comprehensive Viva – Voce	1
	Total	**75 credits**

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PH216	**APPLIED MATHEMATICS FOR ELECTRONIC ENGINEERS** *(Common to M.E. Communication Systems and M.E. Applied Electronics)*	**3**	**2**	**0**	**4**

Course Objectives :

- *To provide strong foundation to the students to expose various emerging new areas of applied mathematics and appraise them with their relevance in Engineering and Technological field.*
- *To develop the ability to use the concepts of Linear algebra and Special functions for solving problems related to Networks.*
- *To formulate and construct a mathematical model for a linear programming problem in real life situation*
- *To expose the students to solve ordinary differential equations by various techniques.*

Course pre-requisites: *Mathematics – III, Probability Theory and Random Process*

Module- I VECTOR SPACES AND CHARACTERISTIC EQUATION (9)

Set Theory (Concept only)- Abelian Group- Examples- Rings and Fields – Properties (statement only) – N-dimensional vectors – Vector spaces and sub spaces – Null spaces and Column spaces – Linear transformations – Matrix of linear transformation – Linear Dependent and Independent set of vectors – Basis and Dimensions – Rank – Real symmetric matrix – Characteristic equation- Eigen values and Eigen vectors of real symmetric matrix

Module – II INNER PRODUCT SPACES AND SPECIAL FUNCTIONS (9)

Inner product spaces – Properties – Examples- Length and Orthogonality- Orthogonal sets- Orthogonal projections- Gram-Schmidt Orthogonalization Process.

Bessel's equation – Bessel Functions – Recurrence relations – generating functions and orthogonal property for Bessel functions.

Module - III OPTIMIZATION TECHNIQUES (9)

Linear Programming Problem- Simplex Method- Variants of Simplex method- Transportation problem- Maximization and Minimization types- Initial basic feasible solution by NWC,LCM and VAM methods – Assignment problem- Hungarian Algorithm for Optimum solution- Travelling Salesman problem – Maxima and Minima of functions of two variables – Constraint Maxima and Minima – Lagrangian multiplier method.

Module IV - NUMERICAL SOLUTION OF DIFFERENTIAL EQUATIONS (9)
Boundary value problems for ODE – Finite difference methods – Numerical solution of PDE – Solution of Laplace and Poisson equations – Liebmann's iteration process – Solution of heat conduction equation by Schmidt explicit formula and Crank-Nicolson implicit scheme – Solution of wave equation.

Module -V STOCHASTIC MODELS (9)
Random variables (concept only)- Stochastic Process – Introduction – Markov Process and Markov chain – Birth and Death Queuing models – Steady state results: Single and multiple server Queuing models – Queues with finite waiting rooms – Little's Formula – M/G/1 queue (steady state solutions only)

TOTAL HOURS: 45 + 15=60

Course Outcomes:

- *Understand the basic concepts of vector space and characteristic equation.*
- *Familiarize the students with special functions and solve problems associated with engineering applications.*
- *Demonstrate and solve various optimization techniques*
- *Apply numerical analysis techniques to solve differential equations.*
- *Understand the notion of Markov chain and be familiar with some simple infinite state space cases such as birth and death chains.*

REFERENCES:

1. David C Lay, "Linear Algebra and its Applications", Pearson Education Asia, NewDelhi,2003
2. Greweal B.S. "Higher Engineering Mathematics", Khanna Publishers, 2005
3. Sankara Rao.K. "Introduction to Partial Differential Equation ", PHI, 1995.
4. D.Gross and C.M. Harris, "Fundamentals of Queueing Theory", Wiley Student edition, 2004.
5. Kanti Swarup, P.K.Gupta, Man Mohan, "Operations research", Ninth edition, S.Chand, Delhi 2001.

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL401	**STATISTICAL SIGNAL PROCESSING** *(Common to M.E. Communication Systems and M.E. Applied Electronics)*	**3**	**2**	**0**	**4**

Course Objectives :

- *To establish fundamental concepts on signal processing in modern spectral estimation.*
- *To study the adaptive filters and its applications.*
- *To explore the concepts of multirate signal processing by study of DFT, computation and design of Multi rate filters*

Course pre-requisites : *Engineering Mathematics III, Digital Signal Processing*

Module - I DISCRETE RANDOM SIGNAL PROCESSING (9)

Discrete Random Processes- Ensemble averages, stationary processes, Autocorrelation and Autocovariance matrices. Parseval's Theorem, Wiener-Khintchine Relation- Power Spectral Density Periodogram, Spectral Factorization, Filtering random processes. Low Pass Filtering of White Noise. Parameter estimation: Bias and consistency.

Module - II SPECTRUM ESTIMATION (9)

Estimation of spectra from finite duration signals, Non-Parametric Methods-Correlation Method, Periodogram Estimator, Performance Analysis of Estimators -Unbiased, Consistent Estimators-Modified periodogram, Bartlett and Welch methods, Blackman –Tukey method. Minimum variance spectrum estimation. Parametric Methods - AR, MA, ARMA model based spectral estimation. Parameter Estimation -Yule-Walker equations, solutions using Durbin's algorithm

Module - III LINEAR ESTIMATION AND PREDICTION (9)

Linear prediction- Forward and backward predictions, Solutions of the Normal equations-Levinson- Durbin algorithms. Maximum likelihood criterion -Least mean squared error criterion -Wiener filter for filtering and prediction , FIR Wiener filter and Wiener IIR filters ,Discrete Kalman filter.

Module - IV ADAPTIVE FILTERS (9)

FIR adaptive filters -adaptive filter based on steepest descent method-Widrow-Hoff LMS adaptive algorithm, Normalized LMS. Adaptive channel equalization-Adaptive echo cancellation-Adaptive noise cancellation- Adaptive recursive filters (IIR). RLS adaptive filters-exponentially weighted RLS-sliding window RLS.

Module - V MULTIRATE DIGITAL SIGNAL PROCESSING (9)

Mathematical description of change of sampling rate - Interpolation and Decimation, Decimation by an integer factor - Interpolation by an integer factor, Sampling rate conversion by a rational factor, Filter implementation for sampling rate conversion- Direct form FIR structures, Polyphase filter structures, time-variant structures. Multistage implementation of multirate system. Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.

TOTAL HOURS=45+15=60

Course Outcomes:

- *Understand the importance of discrete random processing in DSP and its applications on statistical measures, prediction and estimation.*
- *Understand the basic theories behind parametric and non-parametric methods of spectrum estimation.*
- *Understand the concept of linear prediction and estimation and various filter techniques.*
- *Design LMS and RLS adaptive filters for different applications like signal enhancement, channel equalization.*
- *Acquire knowledge about concept of multi rate signal processing and sample rate conversion.*

REFERENCES:

1. Monson H.Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley and Sons,
1. Inc.,Singapore,Reprint 2008.
2. John G. Proakis, Dimitris G. Manolakis, "Digital Signal Processing", Prentice Hall of India,
2. New Delhi, 2009.
3. Dimitris G.Manolakis et.al.,"Statistical and adaptive signal Processing", McGraw Hill, Newyork,2005.
4. Sophoncles J. Orfanidis, "Optimum Signal Processing", McGraw-Hill, 2007.
5. Simon Haykin, "Adaptive signal processing, next generation solutions", John Wiley and Sons, Inc. ,2010
6. P. Vaidyanathan, "Multirate Systems and Filter Banks", Prentice Hall, 1993.

WEB URLs:

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2. http://www.courses.ece.illinois.edu/ECE551/
3. http://www.et.byu.edu/groups/ece777web/
4. http://www.ee.lamar.edu/gleb/adsp/Lecture%2007%20%20Adaptive%20filtering.pdf
5. http://www.users.abo.fi/htoivone/courses/sbappl/asp_chapter2.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL402	ADVANCED DIGITAL SYSTEMS DESIGN	3	2	0	4

1. ***Course Objectives:***
   - *To learn how to design programmable logic circuits.*
   - *To determine the types of fault that occur in digital circuits.*
   - *To describe and simulate the logic design using VHDL.*

2. ***Course pre-requisites:*** *Digital Electronics*

Module - I SEQUENTIAL CIRCUIT DESIGN (9)

Analysis of Clocked Synchronous Sequential Networks (CSSN)-Modeling of CSSN–State Stable Assignment and Reduction–Design of CSSN–Design of Iterative Circuits – ASM Chart – ASM Realization.

Module - II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN (9)

Analysis of Asynchronous Sequential Circuit (ASC)–Flow Table Reduction–Races in ASC–State Assignment–Problem and the Transition Table–Design of ASC–Static and Dynamic Hazards–Essential Hazards–Data Synchronizers–Designing Vending Machine Controller–Mixed Operating Mode Asynchronous Circuits.

Module – III SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES (9)

EPROM to Realize a Sequential Circuit–Programmable Logic Devices–Designing Synchronous Sequential Circuit using a GAL–EPROM–Realization State machine using PLD –FPGA– Xilinx FPGA– Xilinx 2000-Xilinx 3000

Module – IV FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS (9)

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA– Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

Module – V SYSTEM DESIGN USING VHDL (9)

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits - VHDL Code for – Serial Adder, Binary Multiplier–Binary Divider–complete Sequential Systems – Design of a Simple Microprocessor.

TOTAL HOURS=45+15=60

3. Course Outcomes:

- *Design sequential circuit design*
- *Analyze and design asynchronous sequential digital circuits*
- *Realize sequential circuits and understand synchronous design using programmable devices*
- *Understand the fault diagnosis algorithms and test generation schemes*
- *Design combinational circuits using VHDL*

REFERENCES:

1. Donald G. Givone "Digital principles and Design", Tata McGraw Hill 2003.
2. John M Yarbrough "Digital Logic applications and Design", Thomson Learning, 2001
3. Nripendra N Biswas "Logic Design Theory", Prentice Hall of India, 2005
4. Charles H. Roth Jr. "Digital System Design using VHDL", Thomson Learning, 2008.
5. Navabi.Z, "VHDL Analysis and Modeling of Digital Systems", McGraw International, 1998.
6. Parag K Lala, "Digital System design using PLD", BS Publications, 2009.

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2. http: //www.engr.sjsu.edu/caohuut/EE270/Documents/Lecture05.pdf
3. http: //www.eecg.toronto.edu/~ece1767/notes/pect1.pdf
4. http: //www. ee.sharif.edu/~logic_circuits_t/readings/PLD.pdf
5. http: //www.engr.uconn.edu/~tehrani/teaching/ece3401/lec01.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL403	VLSI DESIGN TECHNIQUES	3	0	0	3

1. ***Course Objectives:***
   - *To learn the MOS transistor theory, operation, fabrication and its characteristics*
   - *To understand the design of CMOS systems.*
   - *To learn the concepts of power estimation and delay calculations in CMOS circuits.*
   - *To learn Verilog HDL programming*

2. ***Course pre-requisites:*** *Digital Electronics, VLSI Design*

Module – I INTRODUCTION TO MOS TECHNOLOGY (9)

An overview of Silicon Semiconductor technology- NMOS fabrication, CMOS fabrication: n-well, p-well - Twin tub and SOI Process- CMOS n well / p well design rules – Stick diagrams - Sheet Resistance – Area capacitance –Driving Large Capacitance loads – propagation delay – Wiring Capacitance. Comparison of MOS with Bipolar Technology

Module – II MOS CIRCUIT DESIGN PROCESS (9)

Basic MOS transistors: symbols, Enhancement mode - Depletion mode transistor operation - Threshold voltage derivation - body effect - Drain current Vs voltage derivation - channel length modulation. NMOS inverter- CMOS inverter - DC Characteristics- Switching Characteristics – Power dissipation, Determination of pull up to pull down ratio for an NMOS inverter. Study of channel length effects

Module – III CMOS LOGIC DESIGN (9)

Pass Transistor and Transmission Gate – static CMOS design, Tri-State Circuits- Pseudo NMOS, and dynamic CMOS logic – Clocked CMOS logic – Pre-charged domino logic - Design of logic gates with different techniques - CMOS clocking styles - pipelined systems.

Module – IV SUBSYSTEM DESIGN (9)

Design of Adders: carry look ahead - carry select - carry save, One/Zero Detector, Comparators, Counters-Binary Counter, Multipliers, Memory elements-Read/Write memory, ROM, Content Addressable Memory, Control – Finite State Machines, Control Logic Implementation.

Module – V VERILOG HARDWARE DESCRIPTION LANGUAGE (9)

Introduction to Verilog HDL, hierarchical modeling concepts, modules and port definitions, task & functions, Test Bench, gate level modeling, data flow modeling, behavioral modeling, digital design with Verilog HDL-Multiplexer, Binary Decoders, priority Encoders, Latches, Flip Flops and Registers.

TOTAL HOURS=45

3. Course Outcomes:

- *Understand different VLSI design processes and layout style*
- *Understand and design various MOS circuits*
- *Understand the CMOS logic design*
- *Design Adders and Counters*
- *Write Verilog code for different combinational and sequential circuits*

REFERENCES:

1. Kamran Eshraghian, Douglas A. Pucknell, 'Essentials of VLSI Circuits and Systems', Prentice Hall of India,2013.
2. John P.Uyemura, 'Introduction to VLSI circuits and systems', John Wiley & Sons, 2012.
3. Neil Weste and Kamran Eshranghian,"Principles of CMOS VLSI Design", Pearson Education ASIA, 2010.
4. Samir Palnitkar, "Verilog HDL, A Guide to Digital Design and Synthesis", Pearson Education, 2nd Edition, Reprint 2010.
5. J.Bhasker, "A Verilog HDL Primer", B.S.Publications, 3rd Edition, 2008.
6. Wayne Wolf "Modern VLSI Design System on chip design," Prentice Hall PTR, 2002.

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1. http: //www.cs.unc.edu/~montek/teaching/spring– 05/lecture– 0.ppt
2. http: //www.vlsitechnology.org
3. http: //www.cmosvlsi.com/lect3.pdf
4. http: //www.asic– world.com/verilog/veritut.html

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL451	ADVANCED VLSI LABORATORY	0	0	3	2

1. ***Course Objectives:***

- To understand different combinational and sequential circuit design.
- To understand various parameters involved in the design of digital circuits.

2. ***Course pre-requisites:*** *Fundamentals of Digital Electronics****:***

LIST OF EXPERIMENTS

A. Front end Design using VHDL

Combinational Logic:

- 4-bit parallel adder
- 4-bit serial adder
- Parallel multipliers
- Multiply Accumulate unit

Sequential logic:

- Multi-bit pre-settable, up/down counters
- FIFO buffer
- Sequence detectors
- Real-time Clock

B. Back end Design using back end software

- 4-bit parallel adder
- 4-bit serial adder
- 4-bit up/down counters
- 3-bit Sequence detectors

TOTAL HOURS=30

3. ***Course Outcomes:***
    - *Understand the Xilinx tool for designing digital circuits*
    - *Analyse the various circuits by implementation in FPGA tool.*
    - *Design of combinational and sequential circuits in different aspects*

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL404	ANALOG INTEGRATED CIRCUIT DESIGN	3	2	0	4

1. ***Course Objectives:***
   - *To design the single stage amplifiers using PMOS and NMOS driver circuits with different loads.*
   - *To analyze high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.*
   - *To study the different types of current mirrors and to know the concepts of voltage and current reference circuits.*

2. ***Course pre-requisites:*** *Solid State Circuit-I , Solid State Circuit-II, Linear Integrated Circuits*

Module - I SINGLE STAGE AMPLIFIERS (9)

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads

Module – II FREQUENCY RESPONSE AND NOISE ANALYSIS (9)

Miller effect, Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

Module – III OPERATIONAL AMPLIFIERS (9)

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

Module – IV STABILITY AND FREQUENCY COMPENSATION (9)

General considerations, Multi-pole systems, Phase Margin, Frequency Compensation, compensation of two stage Op Amps, Slewing in two stage Op Amps, other compensation techniques.

Module – V BIASING CIRCUITS (9)

Basic current mirrors, Cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL HOURS=45+15=60

3. Course Outcomes:

- *Analyze single stage amplifiers with MOS loads*
- *Understand the concepts of frequency response and noise characteristics of differential amplifiers*
- *Design and model different active devices with OPAMPs*
- *Describe the multi-pole systems, frequency compensations techniques*
- *Design analog circuits using CMOS technology*

REFERENCES:

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", 5th Edition, Wiley, 2009.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001
3. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.
4. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & Sons Inc., 2003.
5. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002

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2. http: //www.ulb.tu– darmstadt.de/tocs/212596276.pdf
3. http: //www ece.ut.ac.ir/Classpages/S86/ECE089/Chapter1_4in1.pdf
4. http: //www.aicdesign.org/scnotes/2002notes/Chapter02– 2UP(8_13_02).pdf
5. http: //www.granitesemi.com/analogdesign.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL405	DIGITAL CONTROL ENGINEERING	3	2	0	4

1. ***Course Objectives:***
   - *To study the principles of PI, PD, PID controllers.*
   - *To analyze time and frequency response of discrete time control system.*
   - *To familiarize and practice digital control algorithms*

2. ***Course pre-requisites:*** *Control Systems*

Module – I INTRODUCTION (9)

Overview of frequency and time response analysis and specifications of control systems-Digital control systems–basic concepts of sampled data control systems–principle of sampling, quantization and coding–Reconstruction of signals–Sample and Hold circuits–Practical aspects of choice of sampling rate–Basic discrete time signals–Time domain models for discrete time systems.

Module – II MODELS OF DIGITAL CONTROL DEVICES AND SYSTEMS (9)

Z domain description of sampled continuous time plants – models of A/D and D/A converters – Z Domain description of systems with dead time – Implementation of digital controllers – Digital PID controllers –Position, velocity algorithms – Tuning – Zeigler – Nichols tuning method.

Module – III STATE VARIABLE ANALYSIS (9)

State space representation of discrete time systems – Solution of discrete time state space equation – State transition matrix – Decomposition techniques – Controllability and Observability – Multi variable discrete systems.

Module – IV STABILITY ANALYSIS (9)

Mapping of S plane and Z plane- Jury's stability test - Bilinear transformation and extended Routh array- Root Locus Method –Liapunov Stability Analysis of discrete time systems.

Module – V DESIGN OF DIGITAL CONTROL SYSTEM (9)

Z plane specifications of control system design – Digital compensator design – Frequency response method - State feedback – Pole placement design – State Observers – Digital filter properties – Frequency response – Kalman’s filter.

TOTAL HOURS= 45+15=60

3. Course Outcomes:

- *Understand the time and frequency response specifications of control systems*
- *Design Feedback Control Systems*
- *Analyze the state space representation of discrete time systems*
- *Understand the concepts of the Stability in the Frequency Domain*
- *Design the digital control system*

REFERENCES:

1. Gopal M. " Digital Control and State Variable methods-conventional and Neuro-Fuzzy Control Systems", Tata McGraw Hill Publishing Company Ltd., New Delhi, India, Reprint 2010.
2. Kuo B.C. " Digital Control Systems", Oxford University Press, Inc., 2003,Reprint 2011
3. Ogata K, "Discrete Time Control Systems", Prentice Hall International, New Jersey, USA, 2005.
4. Houpis C.H. and Lamont C.B., "Digital Control Systems", Tata McGraw Hill, New Delhi, India, 1999.
5. George V.I;Kurian CP "Digital Control Systems", Cengage Learning,2012

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2. http://www.nptel.ac.in/downloads/108103008/
3. http://www.idsc.ethz.ch/education/lectures/digital-control-systems.html
4. http://nptel.ac.in/courses/108103008/PDF/module3/m3_lec1.pdf
5. https://www.site.uottawa.ca/~rhabash/ELG4152L305.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL406	EMBEDDED SYSTEMS DESIGN	3	2	0	4

1. ***Course Objectives:***
   - *To give sufficient background for understanding embedded systems design.*
   - *To introduce the concepts of embedded systems, its hardware and software.*
   - *To introduce devices and buses used for embedded networking.*
   - *To learn the real time Characteristics and System design techniques.*

2. ***Course pre-requisites:*** *Microprocessor and Microcontrollers*

Module – I EMBEDDED ARCHITECTURE (9)

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioral Description, Design Example: Model Train Controller

Module – II ARM PROCESSOR (9)

Introduction– Implementation-3 stage and 5 stage pipeline ARM organization- Architecture: ARM7 TDMI-ARM8 TDMI-ARM9 TDMI- ARM Instruction Set – The Thumb Instruction Set. Thumb implementation-Thumb applications-Writing simple assembly language programs.

Module – III NETWORKS (9)

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I2C, CAN Bus, SHARC link ports, Ethernet, Myrinet, Internet, Network-Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

Module – IV REAL TIME OPERATING SYSTEMS (9)

Features of Operating Systems - Introduction to real time operating systems - Tasks – Semaphores - Message queues – Pipes - Event registers – Signals - Condition Variables - Case Study of programming – Tasks scheduling – semaphores - queues with Micro C/OS-II.

Module – V REAL-TIME CHARACTERISTICS (9)

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

TOTAL HOURS=45+15=60

3. Course Outcomes:

- *Understand the architecture and design involved in design of embedded systems*
- *Program ARM processor*
- *Understand the embedded system network architecture*
- *Analyze the problems in real time implementation of embedded systems and its solutions*
- *Understand the concepts of system design technologies*

REFERENCES:

1. Wayne Wolf, "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers, 2008.
2. Jane.W.S. Liu," Real-Time Systems", Pearson Education Asia, 2000.
3. C. M. Krishna and K. G. Shin, "Real-Time Systems", McGraw-Hill, 1997.
4. Frank Vahid and Tony Givargi," Embedded System Design: A UnifieHardware/Software Introduction", John Wiley & Sons, 2000.

WEB URLs:

1. http://www.users.ece.gatech.edu/~dblough/8823/embedded_security.pdf
2. http://www.ict.kth.se/courses/IL2206/1011/.../IL2206-L04-Platform_Buses.pdf
3. http://www.dauniv.ac.in/downloads/...PPTs/Chap_3Lesson02EmsysNew.pdf
4. http://www.cs.queensu.ca/home/akl/techreports/scheduling.pdf
5. http://www.cs.colorado.edu/~kena/classes/5828/s10/.../softwaredesign.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL452	EMBEDDED SYSTEMS LABORATORY	0	0	3	2

1. ***Course Objectives:***

- *To understand the working of LCD, UART, Seven segment display and stepper motor.*
- *To understand the programming of Real Time Operating Systems.*
- *To understand the IDE tools used for controller programming and debugging*.

2. ***Course pre-requisites:*** *Fundamentals of microcontrollers Assembly level and C programming.*

LIST OF EXPERIMENTS

1. Board development using 8051 microcontroller
2. Assembly and High level language programs for 8051 - ports - timers - Seven Segment display – UART – LCD interface
3. RTOS – Simple task creation, Round Robin Scheduling, Preemptive scheduling, Semaphores, Mailboxes.
4. Assembly and High level language programs for R8C-ports-timers-Seven segment display – UART – LCD interface – Stepper Motor control
5. Assembly and High level language programs for MSP 430 - ports – timers - Seven Segment display – UART – LCD interface – Stepper Motor control

TOTAL HOURS=30

3. ***Course Outcomes:***

- *Understand the Keil IDE for programming the microcontroller in different aspects.*
- *Understand the functionalities of timer and counter in microcontrollers.*
- *To know the procedure to interface UART, LCD, Seven segment displays, Motors.*
- *Understand the Task creation, Queue and scheduling methods in RTOS.*

PROGRAM ELECTIVES (PE)

PE GROUP 1 – EMBEDDED SYSTEMS

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL601	**HIGH PERFORMANCE MICROPROCESSORS AND MICROCONTROLLERS**	**3**	**0**	**0**	**3**

1. ***Course Objectives:***
   - *To learn the architecture and programming of advanced Intel family microprocessors and microcontrollers.*
   - *To introduce the basic architecture of Pentium family of processors.*
   - *To introduce the architecture programming and interfacing of* MOTOROLA 68HC11 *microcontrollers and architecture of RISC processor and ARM.*

2. ***Course pre-requisites:*** *Microprocessors and Microcontrollers*

Module – I MICROPROCESSOR ARCHITECTURE (9)

Instruction set –Data formats–Instruction formats–Addressing modes–Memory hierarchy–register file–Cache–Virtual memory and paging–Segmentation–Pipelining–instruction pipeline–pipeline hazards–Instruction level parallelism–reduced instruction set–Computer principles–RISC versus CISC–RISC properties–RISC evaluation–On-chip register files versus cache evaluation

Module – II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM (9)

Software model–functional description–CPU pin descriptions–RISC concepts–bus operations – Super scalar architecture–pipe lining–Branch prediction– The instruction and caches– Floating point unit–protected mode operation–Segmentation–paging–Protection–multitasking–Exception and interrupts – Input /Output – Virtual 8086 model – Interrupt processing -Instruction types – Addressing modes – Processor flags – Instruction set -programming the Pentium processor.

Module – III HIGH PERFORMANCE RISC ARCHITECTURE: ARM (9)

ARM architecture–ARM assembly language program–ARM organization and implementation – The ARM instruction set - The thumb instruction set – ARM CPU cores.

Module – IV MOTOROLA 68HC11 MICROCONTROLLERS (9)

Instructions and addressing modes – operating modes – Hardware reset – Interrupt system – Parallel I/O ports – Flags – Real time clock – Programmable timer – pulse accumulator – serial communication interface–A/D converter–hardware expansion–Assembly language Programming

Module – V PIC MICRO CONTROLLER (9)

CPU architecture–Instruction set-Interrupts–Timers–I/O port expansion–I2C bus for peripheral chip access–A/D converter–UART

TOTAL HOURS=45

3. Course Outcomes:

- *Understand the fundamentals and architecture of microprocessor*
- *Understand the CISC architecture-Pentium*
- *Understand ARM architecture and processors*
- *Describe the fundamentals of Motorola microcontrollers*
- *Know the CPU architecture and details of PIC microcontroller*

REFERENCES:

1. Daniel Tabak, "Advanced Microprocessors", McGraw Hill.Inc., 1996
2. James L. Antonakos, "The Pentium Microprocessor", Pearson Education, 2009.
3. Steve Furber, "ARM System –On –Chip architecture", Addison Wesley, 2001.
4. Gene .H.Miller, " Micro Computer Engineering", Pearson Education, 2015.
5. John .B.Peatman, "Design with PIC Microcontroller", Prentice hall, 1998.
6. James L.Antonakos, "An Introduction to the Intel family of Microprocessors", Pearson Education, 1999.

WEB URLs:

1. http://www.nptel.ac.in/courses/Webcourse-contents/IISc-BANG/Microprocessors%20and%20Microcontrollers/pdf/Lecture_Notes/LNm5.pdf
2. http://nptel.ac.in/courses/Webcourse-contents/IIT-KANPUR/microcontrollers/micro/ui/Course_home4_35.htm
3. https://homepages.thm.de/~hg10013/Lehre/MMS/WS0304_SS04/Ioannis/PDF/arm.pdf
4. https://schoolofelectronics.files.wordpress.com/.../introduction-to-m68hc11
5. r.nmu.org.ua/bitstream/handle/123456789/114184/a31a6c6f5447598cd052e1a7cadbb1f0.pdf?sequence=1
6. www.ocw.nit.edu

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL602	RTOS AND ITS APPLICATIONS	3	0	0	3

1. ***Course Objectives:***
   - *To make students understand the concepts of real time embedded systems.*
   - *To learn the need for RTOS in embedded systems and comparison of different RTOS.*

2. ***Course pre-requisites:*** *Embedded Systems*

Module – I INTRODUCTION (9)

Brief History of OS - Defining RTOS, The Scheduler - Objects, Services - Characteristics of RTOS - Defining a Task - Tasks States and Scheduling - Task Operations – Structure – Synchronization - Communication and Concurrency - Defining Semaphores - Operations and Use - Defining Message - Queue - States - Content and Storage - Operation and use.

Module – II SCHEDULING METHODS (9)

Clock driven Approach - weighted round robin Approach - Priority driven Approach - Dynamic Versus Static systems - effective release times and deadlines - Optimality of the Earliest deadline first (EDF) algorithm - challenges in validating timing constraints in priority driven systems - Off-line Versus On-line scheduling.

Module – III FUNCTIONS OF RTOS (9)

Pipes - Event Registers – Signals - Other Building Blocks - Component Configuration - Basic I/O Concepts - I/O Subsystem. Exceptions - Interrupts and Timers: Exceptions – Interrupts – Applications - Processing of Exceptions and Spurious Interrupts - Real Time Clocks - Programmable Timers - Timer Interrupt Service Routines (ISR) - Soft Timers - Operations.

Module – IV REAL-TIME LINUX (9)

Linux and Real-Time - Real-Time Programming in Linux - Hard Real-time Linux - Building and Debugging - Building the Kernel- Integrated Development Environment - Kernel Debuggers - Embedded Drivers – Board support packages – Introduction to µClinux

Module – V CASE STUDIES OF RTOS (9)

RT Linux, MicroC/OS-II, Vx Works - Embedded Linux - Tiny OS and Basic Concepts of Android OS.

TOTAL HOURS=45

3. Course Outcomes:

- *Understand the concepts of embedded operating systems.*
- *Describe various scheduling mechanisms*
- *Work with μCOS – II version RTOS and Embedded Linux.*
- *Port RTOS into an embedded processor.*
- *Develop applications based on RTOS.*

REFERENCES:

1. Qing Li, "Real-Time Concepts for Embedded Systems", Elsevier - CMP Books, 2003.
2. Jane.W.S. Liu, "Real-Time systems", Pearson Education Asia, 2000.
3. Rajkamal, "Embedded Systems- Architecture, Programming and Design",TMH, 2007.
4. Richard Stevens, "Advanced UNIX Programming", Pearson Education Asia, 6th Edition 2009.
5. Dr.Craig Hollabaugh, "Embedded Linux: Hardware, Software and Interfacing" Pearson Education Asia, 2004.

WEB URLs:

1. http://web.mit.edu/16.070/www/year2001/RTOS27.pdf
2. http://www.freertos.org/about-RTOS.html
3. http://freevideolectures.com/Course/3049/Real-Time-Systems#
4. http://nptel.ac.in/courses/106105036/
5. http://iiscs.wssu.edu/drupal/node/4450
6. http://nptel.ac.in/downloads/106105086/
7. http://www2.fsr.ba/nastava/sven/sven.pdf
8. http://www.dauniv.ac.in/downloads/EmbsysRevEd_PPTs/Chap_9Lesson01EmsysNewRTOSes.pdf
9. http://ptgmedia.pearsoncmg.com/images/9780321637734/samplepages/0321637739.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL603	EMBEDDED C	3	0	0	3

1. ***Course Objectives:***
   - *To study essential embedded language features required for embedded systems programming.*
   - *To study pointers and arrays, bit manipulation, register usage.*
   - *To study real-time constraints to common embedded hardware and software problems.*

2. ***Course pre-requisites:*** *Fundamentals of Computing & C programming*

Module – I PROGRAMMING EMBEDDED SYSTEMS IN C (9)

Introduction to embedded system - Selection of processor - Programming language and Operating system. Introducing the 8051 Microcontroller Family - The external interface of the Standard 8051 - Reset circuits - Clock frequency and performance - Memory issues - Special function registers - I/O pins – Timers – Interrupts - Serial interface.

Module – II READING SWITCHES (9)

Introduction - Basic techniques for reading from port pins - Example: Reading and writing bytes - Example: Reading and writing bits (simple version) -Example: Reading and writing bits (generic version) - the need for pull-up resistors - Dealing with switch bounce - Example: Reading switch inputs (basic code) -Example: Counting goats - various types of motor interfacing.

Module – III ADDING STRUCTURE TO THE CODE (9)

Introduction - Object-oriented programming with C - The Project Header (MAIN.H) - The Port Header (PORT.H) - Example: Restructuring the 'Hello Embedded World' example - Example: Restructuring the goat-counting example - UART programming.

Module – IV MEETING REAL-TIME CONSTRAINTS (9)

Introduction - Creating 'hardware delays' using Timer 0 and Timer 1 - Example: Generating a precise 50 ms delay - Example: Creating a portable hardware delay - The need for 'timeout' mechanisms - Creating loop timeouts - Example: Testing loop timeouts - Example: A more reliable switch interface - Creating hardware timeouts - Example: Testing a hardware timeout - LCD interfacing program.

Module – V CASE STUDY (9)

Intruder Alarm System Introduction - The software architecture - Key software components used in this example - running the program - the software.

TOTAL HOURS=45

3. Course Outcomes:

- *Write code using C language for the given task.*
- *Select hardware and software modules depending on the requirement.*
- *Familiarize with adding structures to the codes*
- *Select timer mode and calculate timing.*
- *Analyze and run various embedded applications*

REFERENCES:

1. Michael J. Pont,"Embedded C", Pearson Education, 2nd Ed.2008
2. Nigel Gardner," PIC micro MCU C-An introduction to programming, The MicrochipPIC in CCS C", CCS Inc., 2nd edition, 2002.

WEB URLs:

1. http://www.learn-c.org/
2. http://www.8051projects.net/wiki/Keil_Embedded_C_Tutorial
3. https://blog.udemy.com/embedded-c-tutorial/
4. http://www.edgefx.in/steps-to-build-embedded-c-programming-tutorial/
5. http://www.eng.auburn.edu/~nelson/courses/elec3040_3050/C%20programming%20for%20embedded%20system%20applications.pdf
6. http://www.embedded.com/electrical-engineer-community/general/4402974/Free-MIT-online-C-programming-course
7. http://freevideolectures.com/Course/2999/Embedded-Systems-I/5
8. http://ir.nmu.org.ua/bitstream/handle/123456789/110776/2adbe2fcfcc9b3fd758f3fac7bde709a.pdf?sequence=1

PE GROUP 2 – VLSI

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL604	CAD OF VLSI CIRCUITS	3	0	0	3

1. ***Course Objectives:***
   - *To design miniaturized VLSI circuits by making extensive use of Computer Aided Design (CAD) VLSI design tool.*
   - *The VLSI design professional needs to have a good understanding of the operation of these CAD VLSI design tools as these are developed primarily for and by the VLSI design professionals.*
   - *As part of the present introductory course, the principles of operation of all the important modules that go into the construction of a complete VLSI CAD tool will be discussed. These include the design flow organization for VLSI, the standard cell based synthesis methodologies for digital VLSI, floor planning and placement principles and related topics will be covered.*

2. ***Course pre-requisites:*** *VLSI Design*

Module – I INTRODUCTION TO VLSI DESIGN (9)

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools-Algorithmic Graph Theory and Computational Complexity-Tractable and Intractable problems-general purpose methods for combinatorial optimization.

Module – II LAYOUT (9)

Layout Compaction-Design rules- problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

Module – III FLOOR PLAN (9)

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

Module – IV SIMULATION AND MODELING (9)

Simulation-Gate-level modeling and simulation-Switch-level modeling and simulation-combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

Module – V HIGH LEVEL MODELLING (9)

High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.

TOTALHOURS= 45

3. Course Outcomes:

- *Understand the VLSI design methodologies and the concept behind the combinatorial optimization*
- *Understanding the various types of graph model, layouts and data structure algorithms*
- *Develop problem solving skills for partitioning and routing algorithms*
- *Understand and simulate the modeling levels*
- *Develop problem solving skills in synthesis process*

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
3. Drechsler, R.," Evolutionary Algorithms for VLSI CAD", Kluwer Academic Publishers, Boston, 1998.
4. Hill, D., D. Shugard, J. Fishburn and K. Keutzer," Algorithms and Techniques for VLSI Layout Synthesis", Kluwer Academic Publishers, Boston, 1989.

WEB URLs:

1. http://nptel.ac.in/courses/IIT-MADRAS/CAD_for_VLSI_Design_I
2. http://cdn.intechopen.com/pdfs-wm/26726.pdf
3. http://www.smdp2vlsi.gov.in/smdp2vlsi/downloads/RS_trends-method-cad1.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL605	TESTING OF VLSI CIRCUITS	3	0	0	3

1. ***Course Objectives:***
   - *To understand the concepts of testing, fault models and types of simulations.*
   - *To acquire knowledge in generation of test vectors for combinational and sequential circuits.*
   - *To understand the concepts behind testable design, BIST and fault diagnosis.*

2. ***Course pre-requisites:*** *VLSI Design*

Module – I INTRODUCTION TO TESTING (9)

Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models – Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models -Gate level Event-driven simulation.

Module – II TESTING SEQUENTIAL AND COMBINATIONAL CIRCUITS (9)

Test generation for combinational logic circuits - Testable combinational logic circuit design – Test generation for sequential circuits - design of testable sequential circuits.

Module – III TESTING APPROACHES (9)

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design – System level DFT approaches.

Module – IV BIST (9)

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures – Testable Memory Design - Test algorithms - Test generation for Embedded RAMs

Module – V DIAGNOSIS (9)

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits – Self checking design - System Level Diagnosis.

TOTAL HOURS=45

3. ***Course Outcomes:***

   - *Know about importance of testing and its types in VLSI circuits.*
   - *Understand the testing of sequential and combinational circuits*
   - *Model different faults and carry out fault simulation in digital circuits.*

- *Ability to determine fault oriented test vectors for single stuck-at-faults in combinational and Sequential circuits.*
- *Ability to design digital VLSI circuits with DFT and BIST techniques.*

REFERENCES:

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems Testing and Testability Design", Jaico Publishing House, 2002.
2. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
3. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers, 2002.
4. A.L. Crouch, "Design for Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.

WEB URLs:

1. http://nptel.ac.in/courses/106103116/
2. http://www.eetimes.com/document.asp?doc_id=1216758
3. http://www.asic.co.in/ppt/BIST2.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL606	SYSTEM ON CHIP DESIGN	3	0	0	3

1. ***Course Objectives:***
   - *To learn the principles of SOC design methodology and system-level design of complex SOC*
   - *To understand the importance of co-ware design*
   - *To study the principles of software modelling and hardware implementation*
   - *To design advanced processors in system-on-chip*

2. ***Course pre-requisites :****Embedded systems, C and C++ programming languages, Microprocessor and microcontrollers, Pipelining in ARM processor.*

Module – I SOC DESIGN METHODOLOGY (9)

Introduction, Hardware System Structure, Software Structure, SOC Design Flow, Impact of Semiconductor Economics, Major Issues in SOC Design, Accelerating Processors for Traditional Software Tasks, System Design with Multiple Processors

Module – II SYSTEM-LEVEL DESIGN OF COMPLEX SOC (9)

Complex SOC System Architecture, Processor-Centric SOC Organization: ARM 7 and ARM, Communication Design using Software Mode, Hardware Interconnect Mechanisms, Performance-Driven Communication Design, Non-Processor Building Blocks in Complex SOC system Architecture

Module – III CONFIGURABLE PROCESSOR DESIGN: SOFTWARE APPROACH (9)

Introduction to SystemC, Processor Hardware and Software Cogeneration, Process of Instruction Definition and Application Tuning , The Basics of Instruction Extension, Programmer's Model, Processor Performance Factors

Module – IV CONFIGURABLE PROCESSOR DESIGN: HARDWARE APPROACH (9)

Introduction to Configurable Processors, Introduction to Pipelines and Processors, Hardware Blocks to Processors, Designing the Processor Interface, Hardware Implementation, Verification Flow, Validation and Testing

Module – V ADVANCED TOPICS IN SOC DESIGN (9)

Pipelining for Processor Performance, Processor Pipeline Stalls, Optimizing Processors to Match Hardware, Multiple Processor Debug and Trace, Issues in Memory Systems

TOTAL HOURS: 45

3. Course Outcome:

- *Understand the difference of circuit-level and system-level design*
- *Familiarize about Systems*
- *Design any complex System-on-Chip module*
- *Understand the hardware approach for configurable processors*
- *Learn some of the recent trends in SOC design*

REFERENCES:

1. Wayne Wolf, "Modern VLSI Design – System – on – Chip Design", Prentice Hall, 3rd Edition2008
2. S. Furber, ARM System-on-Chip Architecture, Second Edition, AW, 2000.
3. C. Rowen, Engineering the Complex SOC: Fast, Flexible Design with Configurable Processors, Prentice Hall, 2004.
4. M. Keating, R. J. Rickford and P. Bricaud, Reuse Methodology Manual for System-on-a-Chip Designs, Third Edition, Springer, 2006.
5. D. Black, J. Donovan, SystemC: From the Ground Up, Springer, 2004.
6. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification, Springer, 2009.

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3. http://www.csit-sun.pub.ro/courses/vlsi/Modern_VLSI_Design.pdf
4. http://www.cl.cam.ac.uk/teaching/1011/SysOnChip/socdam-notes1011.pdf
5. http://electro.fisica.unlp.edu.ar/arq/downloads/Papers/ARM/Addison%20Wesley%20-%20ARM%20System-on-Chip%20Architecture,%202Ed.pdf
6. http://cs.anu.edu.au/courses/ENGN3213/lectures/lectures16_17_ARM.pdf
7. http://www.cc.gatech.edu/~hyesoon/spr10/lec_arm.pdf
8. http://freevideolectures.com/Course/2341/Embedded-Systems/10

PE GROUP 3 – DEVICE MODELING

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL607	MEMS AND ITS APPLICATIONS	3	0	0	3

1. ***Course Objectives:***
   - *To introduce the concepts of micro electro mechanical devices.*
   - *To know the fabrication process of Microsystems.*
   - *To know the design concepts of micro sensors and micro actuators.*
   - *To introduce the concepts of quantum mechanics and nano systems.*

2. ***Course pre-requisites:*** *Electron Devices, Physics*

Module – I OVERVIEW AND INTRODUCTION (9)

New trends in Engineering and Science: Micro and Nanoscale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Microelectromechanical Systems, Applications of Micro and Nanoelectromechanical systems, Microelectromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals

Module – II MEMS FABRICATION TECHNOLOGIES (9)

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

Module – III MICRO SENSORS (9)

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor

Module – IV MICRO ACTUATORS (9)

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

Module – V NANOSYSTEMS AND QUANTUM MECHANICS (9)

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL HOURS=45

3. Course Outcomes:

- *Understand the recent trends in engineering and science related to MEMS*
- *Understand the fabrication methods of MEMS devices*
- *Know the design and architecture of Micro machined actuators and sensors*
- *Acquire the fundamentals knowledge of various types of actuator and solve problem related to various design issues.*
- *Describe the fundamentals of nano systems and quantum mechanics*

REFERENCES:

1. Marc Madou, "Fundamentals of Microfabrication", CRC press 1997.
2. Stephen D. Senturia," Micro system Design", Kluwer Academic Publishers, 2001
3. Tai Ran Hsu,"MEMS and Microsystems Design and Manufacture", Tata McGraw Hill, 2002.
4. Chang Liu, "Foundations of MEMS", Pearson education India limited, 2006,
5. Sergey Edward Lyshevski, "MEMS and NEMS: Systems, Devices, and Structures" CRC Press, 2002.
6. 6.Minhang Bao, "Analysis and Design Principles of MEMS Devices", Elsevier ,2005.

WEB URLs:

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2. http://nptel.ac.in/courses/117105082/27
3. http://www.mems-exchange.org/MEMS/what-is.html
4. http://www-bsac.eecs.berkeley.edu/projects/ee245/index.htm
5. http://www.colorado.edu/MCEN/mems/links.htm

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL608	NANO ELECTRONIC DEVICES	3	0	0	3

1. ***Course Objectives:***
   - *To learn and understand basic concepts of Nano electronics.*
   - *To know the techniques of fabrication and measurement.*
   - *To gain knowledge about Nanostructure devices and logic devices.*
   - *To acquire knowledge about fundamental quantum mechanics.*

2. ***Course pre-requisites:*** *Electron Devices*

Module – I INTRODUCTION TO NANOELECTRONICS (9)

Microelectronics towards biomolecule electronics-Particles and waves-Wave-particle duality-Wave mechanics-Schrödinger wave equation- Wave mechanics of particles: Atoms and atomic orbit-Materials for nanoelectronics-Semiconductors-Crystal lattices: Bonding in crystals-Electron energy bands- Semiconductor heterostructures- Lattice-matched and pseudomorphic -Inorganic-organic heterostructures-Carbon nanomaterials: nanotubes and fullerenes

Module – II FABRICATION AND MEASUREMENT TECHNIQUES (9)

Growth, fabrication, and measurement techniques for nanostructures- Bulk crystal and heterostructure growth- Nanolithography, etching, and other means for fabrication of nanostructures and nanodevices- Techniques for characterization of nanostructures- Spontaneous formation and ordering of nanostructures- Clusters and nanocrystals- Methods of nanotube growth- Chemical and biological methods for nanoscale fabrication- Fabrication of nano-electromechanical systems

Module – III PROPERTIES (9)

Dielectrics-Ferroelectrics-Electronic Properties and Quantum Effects-Organic Molecules – Electronic Structures, Properties, and Reactions-Neurons – The Molecular Basis of their Electrical Excitability-Circuit and System Design- Analysis by Diffraction and Fluorescence Methods-Scanning Probe Techniques

Module – IV NANO STRUCTURE DEVICES (9)

Electron transport in semiconductors and nanostructures- Time and length scales of the electrons in solids- Statistics of the electrons in solids and nanostructures- Density of states of electrons in nanostructures- Electron transport in nanostructures-Electrons in traditional low-dimensional structures- Electrons in quantum wells- Electrons in quantum wires- Electrons in quantum dots-Nanostructure devices- Resonant-tunneling diodes- Field-effect transistors- Single-electron-transfer devices- Potential-effect transistors- Light-emitting diodes and lasers- Nano-electromechanical system devices- Quantum-dot cellular automata

Module – V LOGIC DEVICES AND APPLICATIONS (9)

Logic Devices-Silicon MOSFETs-Ferroelectric Field Effect Transistors-Quantum Transport Devices Based on Resonant Tunneling-Single-Electron Devices for Logic Applications-Superconductor Digital Electronics-Quantum Computing Using Superconductors-Carbon Nanotubes for Data Processing- Molecular Electronics

TOTAL HOURS: 45

3. Course Outcomes:

- *Analyse the different types of Nano Structures.*
- *Understand the different nano device fabrication technology.*
- *Learn various characterization techniques.*
- *Identification of new areas of nanodevice application.*

REFERENCES:

1. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications", Cambridge University Press 2011.
2. George W. Hanson,"Fundamentals of Nanoelectronics", Pearson 2009.
3. Mircea Dragoman, Daniela Dragoman, "Nanoelectronics: principles and devices", CRC Press 2006.
4. Mark A. Reed, Takhee Lee,"Molecular nanoelectronics", American Scientific Publishers 2003**.**
5. Jaap Hoekstra, "Introduction to Nanoelectronic Single-Electron Circuit Design", Pan Stanford Publishing 2010**.**
6. W. Ranier, "Nano Electronics and Information Technology", John Wiley & Sons 2012.

WEB URLs:

1. http://nptel.ac.in/courses/115103038/81.
2. 701 Introduction to Nanoelectronics,Complete course notes-http://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-701-introduction-to-nanoelectronics-spring-2010/readings/MIT6_701S10_notes.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL609	SOLID STATE DEVICE MODELING AND SIMULATION	3	0	0	3

1. Course Objectives:

- *To acquaint the students with fundamentals of building device and circuit simulators, and efficient use of simulators.*
- *To study the BJT modelling and know the parameters*
- *To learn about MOSFET modelling*
- *To learn opto-device modelling*

2. ***Course pre-requisites:*** *Solid state circuits-I*

Module – I MOSFET DEVICE PHYSICS (9)

MOSFET capacitor-Basic operation-Basic modeling-Advanced MOSFET modeling- RF modeling of MOS transistors-Equivalent circuit representation of MOS transistor-High frequency behavior of MOS transistor and A.C small signal modeling-model parameter extraction-modeling parasitic BJT-Resistors-Capacitors- Inductors.

Module – II NOISE MODELING (9)

Noise sources in MOSFET- Flicker noise modeling- Thermal noise modeling- model for accurate distortion analysis-nonlinearities in CMOS devices and modeling- calculation of distortion in analog CMOS circuits.

Module – III BSIM4 MOSFET MODELING (9)

Gate dielectric model- Enhanced model for effective DC and AC channel length and width-Threshold voltage model- Channel charge model- mobility model- Source/drain resistance model- I-V model, gate tunneling current model- substrate current models-Capacitance models-High speed model- RF model-noise model- junction diode models- Layout-dependent parasitic model

Module – IV OTHER MOSFET MODELS (9)

The EKV model- model features- long channel drain current model- modeling second order effects of the drain current- modeling of charge storage effects- Non-quasi-static modeling-noise model temperature effects- MOS model 9-MOSAI model.

Module–V MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE (9)

Influence of process variation- modeling of device mismatch for Analog/RF Applications- Benchmark circuits for quality assurance- Automation of the tests.

TOTAL HOURS: 45

3. Course Outcomes:

- *Model BJT and measure the parameters*
- *Model MOSFET and measure the parameters*
- *Model opto devices*
- *Understand noise modelling*
- *Understand BSIM4 MOSFET modelling*

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2003.
2. Arora, N., "MOSFET Models for VLSI Circuit Simulation", Springer-Verlag, 1993
3. Selberherr, S., "Analysis and Simulation of Semiconductor Devices", Springer-Verlag, 1984
4. Fjeldly, T., Yetterdal, T. and Shur, M., "Introduction to Device Modeling and Circuit Simulation", Wiley-Interscience., 1997
5. Grasser, T., "Advanced Device Modeling and Simulation", World Scientific Publishing Company, 2003
6. Donald A. Neaman, " Semiconductor physicsand devices" Third Edition, McGraw –Hill Pvt.Ltd,2007

WEB URLs:

1. http://www.asc.tuwien.ac.at/~juengel/scripts/semicond.pdf
2. http://www.iacs.res.in/ijp/ijp_january_06_rev.pdf

PE GROUP 4 – INSTRUMENTATION AND CONTROL

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL610	ELECTRONIC INSTRUMENTATION	3	0	0	3

1. Course Objectives:

- *To introduce different types of electronic voltmeters and their applications.*
- *To provide knowledge on various types of cathode ray oscilloscopes, their applications and different types of signal analyzers.*
- *To introduce different types of waveform generators and analyzers and their applications.*
- *To educate on virtual instrumentation, its applications, programming and DAQ cards and modules.*
- *To give exposure to telemetry, modulation techniques and multiplexing.*

***2. Course Pre-requisites**: Basic knowledge in electrical and electronics.*

Module –I ELECTRONIC INSTRUMENTS (9)

Electronic Voltmeter and their advantages –Types, Differential amplifier, source Follower, Rectifier–True rms reading voltmeter –Electronic multimeter and ohmmeter – Current measurement –Power measurement -Microprocessor based DMM with auto ranging and self diagnostic features

Module –II CATHODE RAY OSCILLOSCOPE & SIGNAL ANALYZERS (9)

General purpose cathode ray oscilloscope –Dual trace, dual beam and sampling Oscilloscopes – Analog and digital storage oscilloscope - frequency selective and heterodyne wave analyzer – Harmonic distortion analyzer – Spectrum analyzer.

Module –III WAVEFORM GENERATORS (9)

Wien's bridge and phase shift oscillators – Hartley and crystal oscillators – Square wave and pulse generators –Triangular wave-shape generator -Signal and function generators –Q meter – Electronic Counters.

Module –IV VIRTUAL INSTRUMENTATION (9)

Virtual instrumentation (VI) –Definition, flexibility –Block diagram and architecture of virtual instruments –Virtual instruments versus traditional instruments –Software in Virtual Instrumentation -VI programming techniques –DAQ cards for VI applications – DAQ modules with serial communication.

Module –V TELEMETRY (9)

General telemetry system – voltage, current and position telemetry systems – Radio Frequency telemetry – Frequency modulation, pulse-amplitude modulation and pulse - code modulation telemetry – Frequency and time multiplexing.

TOTAL HOURS=45

3. Course Outcomes

- *Understand and analyze Instrumentation systems and their applications to various industries.*
- *Understand and learn the different principles and instruments adopted for measurement of current, voltage, power, energy etc.*
- *Understand different methods available for measurement of passive elements like resistance, inductance & capacitance.*
- *Solve problems in the various electrical parameter measurements.*
- *Study the storage of digital signal and analyzers for analyzing digital signal to provide with meaning full information.*

REFERENCES:

1. A.K. Sawhney, A Course in Electrical & Electronic Measurements and Instrumentation, Dhanpat Rai and Co, New Delhi, 2010
2. Jerome J., Virtual Instrumentation using Lab VIEW, Prentice Hall India Private Ltd., New Delhi, 2010.
3. David A Bell, " Electronic Instrumentation and Measurements", Oxford University Press, 2013.
4. A.D. Helfrick and W.D. Cooper, Modern Electronic Instrumentation and Measurement Techniques, Prentice Hall India Private Ltd., New Delhi, 2010.
5. J.J. Carr, Elements of Electronic Instrumentation and Measurement, Pearson education India, New Delhi, 2011

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2. http://ocw.uc3m.es/tecnologia-electronica/electronic-instrumentation-and-laboratory-of-electronic-instrumentation/lecture-notes-folder/OCW_1_Introduction.pdf
3. http://www.ivt.ntnu.no/imt/courses/tmr7/lecture/Instrumentation.pdf
4. http://old.iihr.uiowa.edu/~hml/people/kruger/Teaching/ece_57018_2008/Lectures/57018_L01.pdf
5. http://lecturenotes.in/notes/engg/aei_3.html

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL611	FAULT TOLERANT SYSTEMS	3	0	0	3

1. ***Course objectives:***
   - *To study about the fundamentals of modeling.*
   - *To understand detection and simulation faults.*
   - *To gain sound knowledge about various testing techniques.*

2. ***Course pre-requisites:*** *Digital Electronics*

Module – I TEST GENERATION FOR DIGITAL SYSTEMS (9)

Introduction – Physical failures and Fault models – Elementary testing concepts – Structural level Test generation – Functional level Test Generation – Random Testing.

Module – II DESIGN FOR TESTABILITY (9)

Introduction – AdHoc techniques – Testability measures - TEMAS, SEOAP, TEST SCREEN. CAMLOT, VICTOR- Scan techniques – Easily testable networks and function independent testing – Built in Self test.

Module – III FAULT SIMULATION (9)

Introduction – Circuit modeling – Logic values – Delays and Timing– User defined description – Circuit capture and expansion – Simulation models for elementary circuits – General simulation algorithm – Evaluation algorithm – Fault modeling – Fault Simulation methods – Parallel, Detective & Concurrent Fault simulation – Data structures at the functional level – fault injection at the functional level – Special Fault simulation problems – comparison of Fault simulation methods – Open issues and directions.

Module – IV CODING THEORY FOR FAULT TOLERANT SYSTEMS (9)

Introduction – Error models – basic structural properties of Parity check codes – Classes of parity check codes and general decoding schemes – Unidirectional and asymmetric codes – Codes for computer memories – Arithmetic codes – On checking Errors in Logical operations – Communication coding .

Module – V CODING TECHNIQUES IN FAULT TOLERANT, SELF-CHECKING AND FAIL-SAFE CIRCUITS (9)

Introduction – Error detection codes and their applications – Self checking circuits – Fault tolerance in Combinational circuits – Fault tolerant Sequential circuits – Fault tolerant asynchronous sequential circuits – Fail safe sequential circuits.

TOTAL HOURS=45

3. ***Course Outcomes:***

- *Understand Software testing and fault tolerant models and their concepts*
- *Using Information redundancy, in error detecting/correcting*
- *Study of quantitative methods for reliability evaluation*
- *Analyze a system for performance-dependability tradeoffs*

REFERENCES:

1. Dhiraj K Pradhan "Fault Tolerant Computing – Theory and techniques", Prentice Hall of India Pvt. Ltd – New Delhi, 1986.
2. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.
3. S.Y. Kung, H.J.Whilo House, T.Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1995.

WEB URLs:

1. https://www.ece.ucsb.edu/Faculty/Parhami/ece_257a.htm
2. http://www2.cs.uidaho.edu/~krings/CS449/

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL612	**NON-LINEAR CONTROL SYSTEM**	**3**	**0**	**0**	**3**

1. ***Course Objectives:***

- *To impart knowledge on phase plane analysis of non-linear systems.*
- *To impart knowledge on Describing function based approach to non-linear systems.*
- *To educate on stability analysis of systems using Lyapunov's theory.*
- *To introduce the concept of sliding mode control.*

2. ***Course Pre-requisites**: Linear Control Systems*

Module-I PHASE PLANE ANALYSIS (9)

Concepts of phase plane analysis-Phase portraits-singular points-Symmetry in phase plane portraits-Constructing Phase Portraits-Phase plane Analysis of Linear and Nonlinear Systems-Simulation of phase portraits in mat lab.

Module – II DESCRIBING FUNCTION (9)

Describing Function Fundamentals-Definitions - Assumptions-Computing Describing Functions-Common Nonlinearities and its Describing Functions - Nyquist Criterion and its Extension-Existence of Limit Cycles-Stability of limit Cycles. Simulation of limit cycles in matlab.

Module – III LYAPUNOV THEORY (9)

Nonlinear Systems and Equilibrium Points - Concepts of Stability-Linearization and Local Stability - Lyapunov's Direct Method - Positive definite Functions and Lyapunov Functions - Equilibrium Point Theorems - Invariant Set Theorems - LTI System Analysis based on Lyapunov's Direct Method - Krasovski's Method - Variable Gradient Method - Physically – Control Design based on Lyapunov's Direct Method.

Module – IV FEEDBACK LINEARIZATION (9)

Feedback Linearization and the Canonical Form - Mathematical Tools – Input - State Linearization of SISO Systems – input - Output Linearization of SISO Systems - Generating a Linear Input - Output Relation - Normal Forms - The Zero – Dynamics - Stabilization and Tracking - Inverse Dynamics and Non – Minimum - Phase Systems - Feedback Linearization of MIMO Systems Zero - Dynamics and Control Design. Simulation of tracking problems in Matlab.

Module – IV SLIDING MODE CONTROL (9)

Sliding Surfaces - Continuous approximations of Switching Control laws - The Modeling/Performance Trade-Offs - MIMO Systems. Simulation of sliding mode controller in matlab.

TOTAL HOURS=45

3. Course Outcomes:

- *Demonstrate knowledge of the effects of non-linearities on the operation of control systems.*
- *Apply the describing function method to nonlinear feedback systems.*
- *Understand the concepts behind Nonlinear Systems and Equilibrium Points*
- *Understand the methods for reducing nonlinear effects in control systems and feedback linearization*
- *Simulate the sliding mode controller*

REFERENCES:

1. J A E Slotine and W Li, Applied Nonlinear control, PHI, 1991.
2. Hasan Khalil, "Nonlinear systems and control", Prentice Hall.
3. S H Zak, "Systems and control", Oxford University Press, 2003.
3 .Torkel Glad and Lennart Ljung, "Control Theory –Multivariable and Nonlinear Methods", Taylor & Francis, 2002.
4 G. J. Thaler, "Automatic control systems", Jaico publishers, 1993
5 Felix L. Chernousko, Igor M.Ananievski, Sergey A.Reshmin, "Control of Nonlinear Dynamical Systems Methods and Applications, Springer, First Indian Reprint 2013.

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1. http://web.mit.edu/nsl/www/videos/lectures.html
2. http://www.nptel.ac.in/courses/108106024/
3. http://freevideolectures.com/Course/2348/Intelligent-Systems-and-Control/5
4. http://web.stanford.edu/class/engr209a/
5. http://www.ioe.nchu.edu.tw/Pic/CourseItem/4497_APPLIED%20NONLINEAR%20CONTROL_slotine_Part1.pdf

PE GROUP 5 – ADVANCED DESIGN

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL613	RF SYSTEM	3	0	0	3

1. ***Course objectives:***

- *To give sufficient background for CMOS based design*
- *To understand the various components that constitute an RF system*
- *To know the basic analysis techniques needed for evaluating the performance of an RF system for various applications*

2. ***Course Pre-requisites :*** *Solid State Circuits-I, Solid State Circuits-II*

Module- I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES (9)

CMOS: Introduction to MOSFET Physics – Noise: Thermal, shot, flicker, popcorn noise Transceiver Specifications: Two port Noise theory, Noise Figure, Sensitivity, SFDR, Phase noise Transceiver Architectures: Receiver: Homodyne, Heterodyne, Image reject, Low IF Architectures – Transmitter: Direct upconversion, Two step upconversion

Module - II IMPEDANCE MATCHING AND AMPLIFIERS (9)

S-parameters with Smith chart – Passive IC components - Impedance matching networks Amplifiers: Common Gate, Common Source Amplifiers – OC Time constants in bandwidth estimation and enhancement – High frequency amplifier design Low Noise Amplifiers: Power match and Noise match – Single ended and Differential LNAs – Terminated with Resistors and Source Degeneration LNAs.

Module - III FEEDBACK SYSTEMS AND POWER AMPLIFIERS (9)

Feedback Systems: Stability of feedback systems: Gain and phase margin, Root-locus techniques –Time and Frequency domain considerations–Compensation, Power Amplifiers: General model –Class A, AB, B, C, D, E and F amplifiers–Linearisation Techniques – Efficiency boosting techniques – ACPR metric.

Module - IV PLL AND FREQUENCY SYNTHESIZERS (9)

PLL: Linearised Model – Noise properties – Phase detectors – Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers – Direct Digital Frequency synthesizers

Module - V MIXERS AND OSCILLATORS (9)

Mixer: characteristics–Non-linear based mixers: Quadratic mixers–Multiplier based mixers: Single balanced and double balanced mixers–subsampling mixers Oscillators: Describing Functions, Colpitts oscillators–Resonators–Tuned Oscillators–Negative resistance oscillators–Phase noise Filter: Basic resonator and filter configurations-special filter realization-filter implementation-coupled filter

TOTAL HOURS:45

3 .*Course Outcomes:*

- *Understand the fundamentals of CMOS architecture and specification*
- *Analyze the performance of RF circuits and design RF circuits*
- *Understand the working concepts of RF active components and amplifiers*
- *Understand the frequency synthesizers and linearised PLL model*
- *Study the operation of mixers and oscillators.*

REFERENCES:

1. T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2. B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3. Jan Crols, Michiel Steyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers, 1997.
4. B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, 2001.
5. Thomas H Lee, J.L. Dawson , “Feedback linearization of RF Power Amplifiers” , Kluwer Publishers 2004.

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2. http://www.seas.ucla.edu/brweb/teaching.html
3. http://nptel.ac.in/courses/117102012/

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL614	SIGNAL INTEGRITY FOR HIGH SPEED DESIGN	3	0	0	3

1. ***Course Objectives:***
   - *To identify sources affecting the speed of digital circuits.*
   - *To introduce methods to improve the signal transmission characteristics*

2. ***Course pre-requisites:*** *Electromagnetics, Transmission Lines and networks*

Module – I SIGNAL PROPAGATION ON TRANSMISSION LINES (9)
Signal Integrity – Importance of Signal Integrity – Electromagnetic Fundamentals – Maxwell's Equation, Wave propagation, Electrostatics, Magnetostatics, Reflections of Electro Magnetic Waves – Transmission Line Fundamentals – Infinite uniform transmission line, Effects of source and load impedance, Special transmission line cases, Line impedance and propagation delay - terminations –per UNIT- length parameters, PCB layer stackups, cross-sectional analysis tools, Zo and Td equations for microstrip and stripline - Reflection and terminations, input impedance, skin-effect.

Module – II MULTI-CONDUCTOR TRANSMISSION LINES AND CROSS-TALK (9)
Multi-conductor transmission-lines, coupling physics, per UNIT- length parameters - Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) - Differential signaling, termination, balanced transmission lines, S-parameters, Lossy and Lossless models

Module – III NON-IDEAL EFFECTS (9)
Non-ideal signal return paths– gaps, , via transitions, Parasitic inductance and capacitance, Transmission line losses - Common-mode current, differential-mode current - Connectors

Module – IV POWER CONSIDERATIONS AND SYSTEM DESIGN (9)
SSN/SSO, SMT decoupling, Power consumption and system power delivery, Logic families and speed Package types and parasitic, SPICE, IBIS models, Eye diagrams , jitter, inter-symbol interference Bit-error rate ,Timing analysis

Module – V CLOCK DISTRIBUTION AND CLOCK OSCILLATORS (9)
Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL HOURS: 45

3. Course Outcomes:

- *Understand the signal propagation on transmission lines*
- *Understand the multi conductor transmission lines*
- *Identify sources affecting the speed of digital circuits.*
- *Analyze the power considerations and timing design*
- *Describe the clock distribution and oscillators*

REFERENCES:

1. H. W. Johnson and M. Graham, "High-Speed Digital Design: A Handbook of Black Magic", Prentice Hall, 1993.
2. Douglas Brooks, "Signal Integrity Issues and Printed Circuit Board Design", Prentice Hall PTR, 2003.
3. S. Hall, G. Hall, and J. McCall, "High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices", Wiley-Interscience, 2000.
4. Stephen H.Hall, Howard L.Heck, "Advanced Signal Integrity for High Speed Design" , Wiley- IEEE Press, 2009.
5. Stephen C. Thierauf, "High-speed Circuit Board Signal Integrity" Artech House, 2004.
6. Clayton R.Paul, "Analysis of Multiconductor Transmission Lines", John Wiley & Sons, 2008.

WEB URLs:

1. www.analog.com/media/en/training-seminars/tutorials/MT-094.pdf
2. https://www.altera.com/content/dam/altera-ww/global/en_US/pdfs/literature/wp/wp_sgnlntgry.pdf
3. https://courses.cs.washington.edu/courses/cse467/11wi/lectures/si_lec1_jandhyala_feb2011.pdf

TOOLS REQUIRED

1. SPICE, source - http://www-cad.eecs.berkeley.edu/Software/software.html

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL615	**ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY** *(Common to M.E. Communication Systems and M.E. Applied Electronics)*	**3**	**0**	**0**	**3**

1. ***Course Objectives:***
   - *To understand the basics of EMI*
   - *To study EMI Sources*
   - *To understand EMI problems*
   - *To understand Solution methods in PCB*
   - *To understand Measurement technique for emission*
   - *To understand Measurement technique for immunity*

2. ***Course Pre-requisites**: EMF*

Module I EMI/EMC CONCEPTS (9)

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

Module- II EMI COUPLING PRINCIPLES (9)

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

Module- III EMI CONTROL TECHNIQUES (9)

Shielding- Shielding Material-Shielding integrity at discontinuities, Filtering- Characteristics of Filters-Impedance and Lumped element filters-Telephone line filter, Power line filter design, Filter installation and Evaluation, Grounding- Measurement of Ground resistance-system grounding for EMI/EMC-Cable shielded grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control. EMI gaskets.

Module- IV EMC DESIGN OF PCBS (9)

EMI Suppression Cables-Absorptive, ribbon cables-Devices-Transient protection hybrid circuits, Component selection and mounting; PCB trace impedance; Routing; Cross talk control-Electromagnetic Pulse-Noise from relays and switches, Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

Module- V EMI MEASUREMENTS AND STANDARDS (9)

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Transmitter /Receiver Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Receiver and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462. Frequency assignment - spectrum conversation. British VDE standards, Euro norms standards in Japan - comparisons. EN Emission and Susceptibility standards and Specifications.

TOTAL HOURS=45

3 . ***Course Outcomes:***

- *Learn the basic concepts of EMI/EMC.*
- *Understand the principles of various EMI coupling methods.*
- *Design and study EMI control techniques.*
- *Design high speed Printed Circuit board with minimum interference*
- *Learn EMI measurements, standards and specifications.*

REFERENCES:

1. V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
2. Clayton R.Paul," Introduction to Electromagnetic Compatibility", John Wiley Publications, 2008
3. Henry W.Ott.,"Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
4. Bemhard Keiser, "Principles of Electromagnetic Compatibility", Artech house, Norwood, 3rd Ed, 1986.
5. Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC", Vol I-V, 1988.

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2. http://www.cvel.clemson.edu/emc/
3. http://www.users.ece.gatech.edu/mleach/ece4391/set1ab.pdf
4. http://www.fda.gov/MedicalDevices/DeviceRegulationandGuidance/GuidanceDocuments/ucm077210.htm
5. http://www.fda.gov/RadiationEmittingProducts/RadiationSafety/Electromagnetic Compatibility EMC/ucm116566.htm

PROGRAM SOFT CORE (PSC)

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL501	PRINCIPLES OF SOFT COMPUTING	3	0	0	3

1. ***Course Objectives:***

- *To learn the key aspects of Soft computing and Neural networks.*
- *To know about the components and building block hypothesis of Genetic algorithm.*
- *To understand the features of neural network and its applications*
- *To study the fuzzy logic components*
- *To gain insight onto Neuro Fuzzy modeling and control.*
- *To gain knowledge in machine learning through Support vector machines.*

2. ***Course pre-requisites:*** *Numerical Methods*

Module – I INTRODUCTION TO SOFT COMPUTING (9)

Evolution of Computing - Soft Computing Constituents – From Conventional AI to Computational Intelligence - Machine Learning Basics

Module – II GENETIC ALGORITHMS (9)

Introduction, Building block hypothesis, working principle, Basic operators and Terminologies like individual, gene, encoding, fitness function and reproduction, Genetic modeling: Significance of Genetic operators, Inheritance operator, cross over, inversion & deletion, mutation operator, Bitwise operator, GA optimization problems, JSPP (Job Shop Scheduling Problem), TSP (Travelling Salesman Problem),Differences & similarities between GA & other traditional methods, Applications of GA.

Module – III NEURAL NETWORKS (9)

Machine Learning using Neural Network, Adaptive Networks – Feed Forward Networks – Supervised Learning Neural Networks – Radial Basis Function Networks - Reinforcement Learning – Unsupervised Learning Neural Networks – Adaptive Resonance Architectures – Advances in Neural Networks.

Module – IV FUZZY LOGIC (9)

Fuzzy Sets–Operations on Fuzzy Sets–Fuzzy Relations–Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making

Module – V NEURO-FUZZY MODELING (9)

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification – Neuro-Fuzzy Control – Case Studies.

TOTAL HOURS=45

3. Course Outcomes:

- *Implement machine learning through Neural networks.*
- *Develop a Fuzzy expert system.*
- *Model Neuro Fuzzy system for clustering and classification.*
- *Write Genetic Algorithm to solve the optimization problem*
- *Use Support Vector Machine for enabling the machine learning*

REFERENCES:

1. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, "Neuro-Fuzzy and Soft Computing",Prentice-Hall of India, 2003.
2. Kwang H.Lee, "First course on Fuzzy Theory and Applications", Springer–Verlag BerlinHeidelberg, 2005.
3. James A. Freeman and David M. Skapura, "Neural networks algorithms, applications, andprogramming techniques", Pearson edn., 2003.
4. David E. Goldberg, "Genetic algorithms in search, optimization and machine learning",Addison wesley, 2007.
5. S.N.Sivanandam, S.N.Deepa, "Introduction To Genetic Algorithms", Springer, 2007.

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2. http://www.cs.cmu.edu/~02317/slides/lec_9.pdf
3. http://nptel.ac.in/courses/117105084/
4. http://www.kau.edu.sa/Files/0052079/Subjects/fuzzy.pdf
5. http://www.uni-obuda.hu/users/fuller.robert/dam.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL502	DESIGN OF LOW POWER VLSI CIRCUITS	3	0	0	3

1. ***Course Objectives:***

- *To learn the various sources of power dissipation and techniques to reduce power*
- *To design low power CMOS circuits and Memories*
- *To learn the various power estimation techniques and software design*

2. ***Course pre-requisites:*** *VLSI Design*

Module – I POWER DISSIPATION IN CMOS (9)

Need for Low Power VLSI Chips – Basic Principles of Low Power Design – Logic Synthesis for Low Power – Hierarchy of Limits of Power– Sources of Power Dissipation – Physics of power dissipation in MOSFET devices.

Module – II POWER OPTIMIZATION (9)

Logical level power optimization – Optimization Algorithms – Circuit level low power design – Circuit techniques for reducing power consumption in adders and multipliers.

Module – III DESIGN OF LOW POWER CMOS CIRCUITS (9)

Computer Arithmetic techniques for low power systems – Low Power SRAM and DRAM Architecture – Reducing power consumption in memories – Low power clock design – Interconnect delays and layout design – Advanced techniques–Special techniques.

Module – IV POWER ESTIMATION (9)

Logic Level Power estimation – Classification of power estimation techniques – Simulation based power analysis – Probabilistic power analysis – Statistical Techniques – Power Estimation at Circuit Level – Estimation of Maximum Power.

Module – V LOW POWER VLSI SYSTEM DESIGN (9)

Behavioral level transforms – Algorithm and Architecture Level Transforms for Low Power – Low power design with multiple supply and threshold voltages – Gated clocking – Software design for low power – Software power estimation and optimization – Co-design for Low Power.

TOTAL HOURS=45

3. ***Course Outcomes:***

- *Identify the sources of power dissipation in digital IC systems. Understand the impact of power on system performance and reliability*
- *Describe various power optimization algorithms in low power VLSI design system*

- *Design of low power CMOS circuits*
- *Apply probabilistic analysis to characterize dynamic power estimation.*
- *Able to design low power VLSI circuits and apply the techniques in different applications.*

REFERENCES:

1. K.Roy and S.C. Prasad ," Low Power CMOS VLSI circuit design", Wiley and sons,2000
2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage , Low-Power VLSI Subsystems", McGraw Hill, 2009.
3. Gary Yeap, "Practical low power digital VLSI design", Kluwer Academic Publishers, 1998.
4. J.B. Kuo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley and sons, 1999.
5. James B. Kuo, Shin – Chia Lin," Low voltage SOI CMOS VLSI Devices and Circuits", John Wiley and sons, 2009.

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4. http://www.powershow.com/view4/55d383-ZjU2O/Lecture_8_Logic_Circuit_Synthesis_for_Low-Power_powerpoint_ppt_presentation

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL503	DESIGN OF APPLICATION SPECIFIC INTEGRATED CIRCUITS	3	0	0	3

1. ***Course Objectives:***
   - *To introduce the concepts of ASIC Design, types of programmable ASIC logic, I/O cells, interconnects, design software and placement and routing*

Module–I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN (9)

Types of ASICs - Design flow - CMOS transistors- CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture

Module–II PROGRAMMABLE ASICS, LOGIC CELLS AND I/O CELLS (9)

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

Module – III PROGRAMMABLE ASIC INTERCONNECT, DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY (9)

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

Module – IV LOGIC SYNTHESIS, SIMULATION AND TESTING (9)

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

Module – V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING (9)

System partition-FPGA partitioning-partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing-circuit extraction - DRC.

TOTAL HOURS:45

2. ***Course Outcomes:***
   - *Understand the basics of ASIC.*
   - *Know the different types of programmable ASIC.*
   - *Understand different types of FPGA and ASIC structures.*

- *Design ASIC for real time applications.*
- *Understand the logic synthesis of Verilog and VHDL*

REFERENCES:

1. M.J.S .Smith, "Application - Specific Integrated Circuits" – Pearson Education India, 1997.
2. Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, "Field Programmable Gate Arrays", Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", McGraw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, "VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

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1. http://www.ece.ncsu.edu/asic/tutorials/tutor1/tutor1.pdf
2. http://www.csee.umbc.edu/~cpatel2/links/641/slides/lect01_flow.pdf
3. http://www2.units.it/marsi/elettronica2/lucidi/UNIVTS_2003_nobak.pdf

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL504	HARDWARE SOFTWARE CO-DESIGN	3	0	0	3

1. ***Course Objectives:***
   - *To introduce the techniques of embedded systems and software- hardware co design*
   - *To introduce the ideas of prototyping and emulation*
   - *To familiarize with design specification and verification*

2. ***Course pre-requisites:*** *Embedded Systems*

Module – I SYSTEM SPECIFICATION AND MODELLING (9)

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modelling, Co-Design for Heterogeneous Implementation-Processor Synthesis, Single-Processor Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi-Processor Architectures , Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification .

Module – II HARDWARE/SOFTWARE PARTITIONING (9)

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the Hardware/Software Partitioning Problem, Optimization, Hardware/Software Partitioning based on Heuristic Scheduling, Hardware/Software Partitioning based on Genetic Algorithms.

Module – III HARDWARE/SOFTWARE CO-SYNTHESIS: (9)

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

Module – IV PROTOTYPING AND EMULATION (9)

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

Module – V DESIGN SPECIFICATION AND VERIFICATION (9)

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation

TOTAL HOURS: 45

3. ***Course Outcomes:***
   - *Implement Hardware Software Co Design*
   - *Familiarize with modern hardware/software tools for building prototypes*
   - *Demonstrate practical competence in these areas.*
   - *Understand the prototyping and emulation*
   - *Describe the design specification and verification*

REFERENCES:

1. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Publishers, 1998.
2. Jorgen Staunstrup, Wayne Wolf,"Hardware/Software Co-Design: Principles and Practice", Kluwer Academic Publishers, 1997.
3. Giovanni De Micheli, Rolf Ernst Morgon,"Reading in Hardware/Software Co-Design", Kaufmann Publishers, 2001.

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3. http://ece.ut.ac.ir/Classpages/S87/ECE612/lectures/4-System%20Partitioning.pdf
4. http://www.modprod.liu.se/workshop_2007/1.46549/tutorial-peng.pdf
5. https://ls12-www.cs.tu-dortmund.de/daes/de/forschung/hwsw-co-design.html

Course Code	Course Name	Contact Hours			
		L	T	P	C
15PL505	RECONFIGURABLE COMPUTING	3	0	0	3

1. ***Course Objectives:***
   - *To understand the need for reconfigurable computing*
   - *To expose the students to various device architectures*
   - *To examine the various reconfigurable computing systems*
   - *To understand the different types of compute models for programming reconfigurable architectures*
   - *To expose the students to HDL programming and familiarize with the development environment*
   - *To expose the students to the various placement and routing protocols*
   - *To develop applications with FPGAs*

2. ***Course pre-requisites:*** *VLSI Design*

Module – I DEVICE ARCHITECTURE (9)

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices –Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.

Module – II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS(9)

Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.

Module – III PROGRAMMING RECONFIGURABLE SYSTEMS (9)

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing –Operating System Support for Reconfigurable Computing.

Module – IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS (9)

The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bitstream Generation – Case Studies with Appropriate Tools.

Module – V APPLICATION DEVELOPMENT WITH FPGAS (9)

Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs.

TOTAL HOURS: 45

3. Course Outcomes:

- *Identify the need for reconfigurable architectures*
- *Discuss the architecture of FPGAs and build basic modules using any HDL*
- *Point out the salient features of different reconfigurable architectures*
- *Develop applications using any HDL and appropriate tools*
- *Design and build an SoPC for a particular application*

REFERENCES:

1. Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
2. Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation", Elsevier / Morgan Kaufmann, 2008.
3. Christophe Bobda, "Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications", Springer, 2010.

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